(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 840 505 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
06.05.1998 Bulletin 1998/19

(51) Int. Cl.[6]: **H04N 5/45**

(21) Application number: **97119124.2**

(22) Date of filing: **03.11.1997**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **01.11.1996 US 30104 P**

(71) Applicant:
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas 75243 (US)

(72) Inventors:
- **Chauvel, Gerard**
  06600 Antibes (FR)
- **Chae, Brian**
  Plano, TX 75075 (US)

(74) Representative: **Holt, Michael**
Texas Instruments Limited,
Kempton Point,
68 Staines Road West
Sunbury-on-Thames, Middlesex TW16 7AX (GB)

(54) System to multiplex and blend graphics OSD and motion video pictures for digital television

(57) A system is provided to multiplex graphic and Motion video pictures for digital TV set-top box. The motion picture is generated by an MPEG Video decoder and the graphic windows are generated by an OSD Co-Processor. Each graphic window is characterized by a set of attributes that define the display mode, position on the screen, priority and blend factor. When a window is blended, the motion video and OSD color components are added together with a proportion of each defined by the window attributes. Decimated motion video picture can be also displayed within an OSD window; the OSD Co-processor generates an empty window that is filled by the video decoder with the decimated motion video.

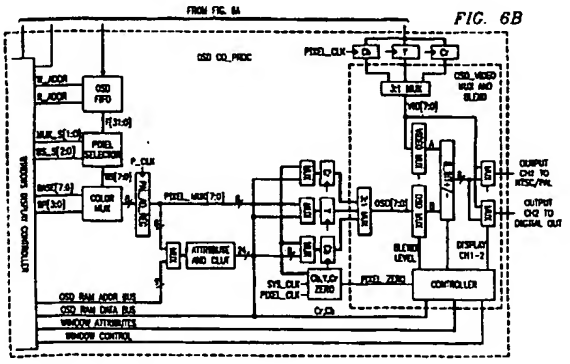


FIG. 6B

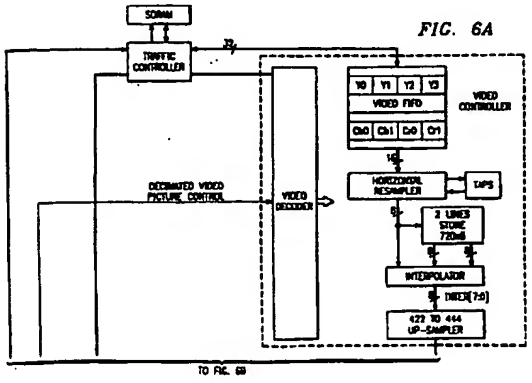


FIG. 6A

EP 0 840 505 A2

Description

FIELD OF THE INVENTION

This invention relates to System to Multiplex and Blend Graphics OSD and Motion Video Pictures for digital television.

BACKGROUND OF THE INVENTION

Digital TV set-top boxes are currently being tested and utilized in some areas. However, these boxes often provide insufficient capabilities for displaying windows.

SUMMARY OF THE INVENTION

A system is provided to multiplex graphic and Motion video pictures for digital TV set-top box. The motion picture is generated by an MPEG Video decoder and the graphic windows are generated by an OSD Co-Processor. Each graphic window is characterized by a set of attributes that define the display mode, position on the screen, priority and blend factor. When a window is blended, the motion video and OSD color components are added together with a proportion of each defined by the window attributes. Decimated motion video picture can be also displayed within an OSD window; the OSD Co-processor generates an empty window that is filled by the video decoder with the decimated motion video.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described, by way of example, with reference to the accompanying drawings in which:

Figure 1 depicts an OSD window blended over video;
Figure 2 illustrates two windows over a full screen background color;
Figure 3 depicts decimated by ½ of motion video pictures;
Figure 4 shows a decimation filter algorithm;
Figure 5 shows video output timings;
Figures 6A and 6B depict the main blocks of a system to multiplex and blend graphic and motion video pictures of the present invention;
Figure 7 shows the timing of OSD outputs in different modes; and
Figure 8 shows of an OSD/video 4 levels blend matrix.

DETAILED DESCRIPTION

The video decoder (Figure 1) decodes MPEG2 data and built the motion video picture into the SDRAM, and display every frame a new picture. The OSD windows can be displayed over the motion video or blended with the video with different levels of blending. The coordinates, size and display attributes of each windows are defined in the window attribute memory. During display the OSD Co_processor read and interprets the OSD data stored within the SDRAM. A window can be: graphic, bit-map, still video or empty. The Figure 1 shows a full screen motion video picture with an OSD window. During the parts of motion video the Luma and Chroma is generated by the video decoder and transmitted to the video output through the input A of the Mux. In a graphic window the Luma and Chroma are generated by the OSD Co-processor through the input B of the Mux. If the window is blended, motion video and graphics are added together with a proportions defined by the window attributes.

Figure 2 contains two windows over a full screen background color. The window 4 contain a graphic, bitmap or still picture and the window 1 contain a motion video picture. The position and size of the each windows are defined by the attributes stored in OSD Co-processor Every frame a picture is read and decimate in real time. The decimation ratio is defined by the window attributes.

Full screen and decimated by ¼ motion video pictures are shown Figure 3 and Figure 4 shows the decimation filter algorithm. The video decoder decimate vertically by reading the source video every two lines. The line n+1 and n+3 are ignored. Horizontally the decimation filter decimate by 2. The number of pixels is reduced horizontally by 2. Pi is generated from Pj and its neighbor Pj-1 and Pj+1. The result of vertical and horizontal decimation is a motion picture 4 time smaller than the original picture. In this example three pixels are used to generate one, more complex filters with 5, 7 or 9 pixels can be used to improve picture quality. Different ratios of decimation are possible: 1/2, 1/3 and 1/4.

Figures 6A and 6B represent the main blocks of the system to multiplex and blend graphic and motion video pictures: the MPEG video decoder and the OSD Co-processor, traffic controller and SDRAM. The data to be displayed are stored in SDRAM, the traffic controller manage the access to the memory.

The video decoder contain several blocks to decode and display the MPEG2 data, they are: RISC CPU, VLD, IDCT, Motion Compensation and video controller Modules. The CPU execute micro-instructions, handle interrupt, control and synchronize modules and schedule traffic to SDRAM. Only the video controller is detailed in Figures 6A and 6B. The CPU manage the transfer from the motion video source picture to the Video FIFO. A 32-bit word contain 4 Luma Y0 to Y3 or 2 chroma samples Cb0, Cr0 and Cb1, Cr1. The transfer between SDRAM and FIFO is done by burst. During the display the video controller access samples in FIFO to generate pixel by pixel the 3 color components: Cb, Y and Cr. To reduce memory space the motion video picture is stored in 4:2:0 format, Chroma resolution is

divided by 2 horizontally and vertically. Chroma is interpolated by the block interpolator that generates the 4:2:2 picture using the current line and 2 previous lines. The polyphase filter required for horizontal re-sampler is implemented in the video data path. The coefficients for the filter are stored in Taps memory. Filters support re-sampling from 360...704 to 720 and horizontal decimation by 2, 3 or 4. The output Inter[7:0] of the interpolator generate each pixel a Luma sample Y and a chroma sample alternately Cb or Cr, output frequency is 27Mhz. The video output is modified in order to be synchronous with the system clock 40.5Mhz. Figure 5 shows the modified video output and the output of the up-sampler. Pixel frequency is 13.5 Mhz.

The OSD Co-processor controls the display of the OSD windows. Each hardware window has the following attributes:

window position: any even pixel horizontal position on screen; windows with decimated video have to start from an even numbered video line also
window size: from 2 to 720 pixel wide (even values only) and 1 to 576 lines
window base address
data format: bitmap, YCrCb 4:4:4, YCrCb 4:2:2, and empty
bitmap resolution: 1, 2, 4, and 8 bits per pixel
full or half resolution for bitmap and YCrCb 4:4:4 windows
bitmap color palette base address
blend enable flag
4 or 16 levels of blending
transparency enable flag for YCrCb 4:4:4 and YCrCb 4:2:2
output channel control

The window position, size and priority are stored in CAM memory located in the window display controller. The window attributes and CLUT are store in attribute memory. The OSD Co-processor manage the transfer between SDRAM and OSD FIFO, line by line and by segments of window to be displayed. Each pixel it generates the color component YCrCb or the CLUT address in bitmap. In graphic 4:4:4 mode, the window memory contain the 3 color components Cb, Y and Cr. In still video 4:2:2 mode the window memory contain the color components Y and alternately Cb, or Cr. In bitmap the window memory contain the code of the color to be displayed, the color components are stored in the CLUT. Figure 7 shows the timing of OSD outputs in different modes. In bit map the code of the color concatenated with the color base address select one of the color of the CLUT. The 3 color components are stored in the respective registers and multiplexed at the system clock frequency to generate Osd[7:0] output.

In 4:2:2 still video, the color components Cr, Y and Cb are transferred to the respective registers. Every 2 pixels only Y is modified. The 3 color components are multiplexed at the system clock frequency to generate Osd[7:0] output.

In 4:4:4 graphic, the color components Cr, Y and Cb are transferred to the respective registers and multiplexed at the system clock frequency to generate Osd[7:0] output.

In Figures 5 and 7, the color components of Vid[7:0] and Osd[7:0] are in phase and can be combined together to blend graphic and video.

When the blend enable attribute is selected the corresponding OSD window is blend over the video. Figure 8 shows a 4 levels blend matrix. The blend level is defined with the window attribute. The OSD output Ch1 and/or Ch2 are:

Full OSD: Output is Osd[7:0]
Full Video: Output is Vid[7:0]
½ Video and ½ OSD: Output is Osd[7:1] + Vid[7:1]
Video and ¼ OSD: Output is Osd[7:2] + Vid[7:1] + Vid[7:2]
¼ Video and ¾ OSD: Output is Osd[7:1] + Osd[7:2] + Vid[7:2]

Blending can be at window or color level. When blending at window level is selected the attributes define the level of blending according to the matrix Figure 8. In bit-map when color level is selected the LSB bit(s) of Cb and Cr are used to select the blend level.

In graphic of still video when blend is enable, the value zero of Cb, Y and Cr indicate a transparent color. The corresponding OSD pixels are replaced with the Vid[7:0]].

Empty window attribute selects a decimated motion picture in an OSD window. During the display the window display controller generate a signal: "Decimated window control" to indicate to the video controller the presence of a decimated window and the decimation ratio. The Video decoder decimate vertically by loading the video FIFO with the selected motion video lines, every 2, 3 or 4 lines depending of the decimation ratio. The horizontal re-sampler decimate horizontally by 2, 3 or 4 with the corresponding decimation filter. Window control and decimated video picture control select the Vid[7:0] output to fill the empty window. The position of the empty window is selected by window attributes.

The attribute output channel control selects the windows to be displayed at the outputs Ch1 and/or Ch2. Each window can be selected independently. When a window is not selected the corresponding area is replaced by the motion video. This system allows to have one channel for VCR recorder that records video and sub-title and the second channel with the full OSD menu.

Claims

1. A system for generating synchronous color components from different display modes comprising:

a video decoder, and

an OSD co-processor,

wherein said display modes are selected from Motion video, 4:2:2, 4:4:4 and bit-map, or combinations thereof.

2. A blending and decimated window system comprising:

a video decoder, and

an OSD co-processor.

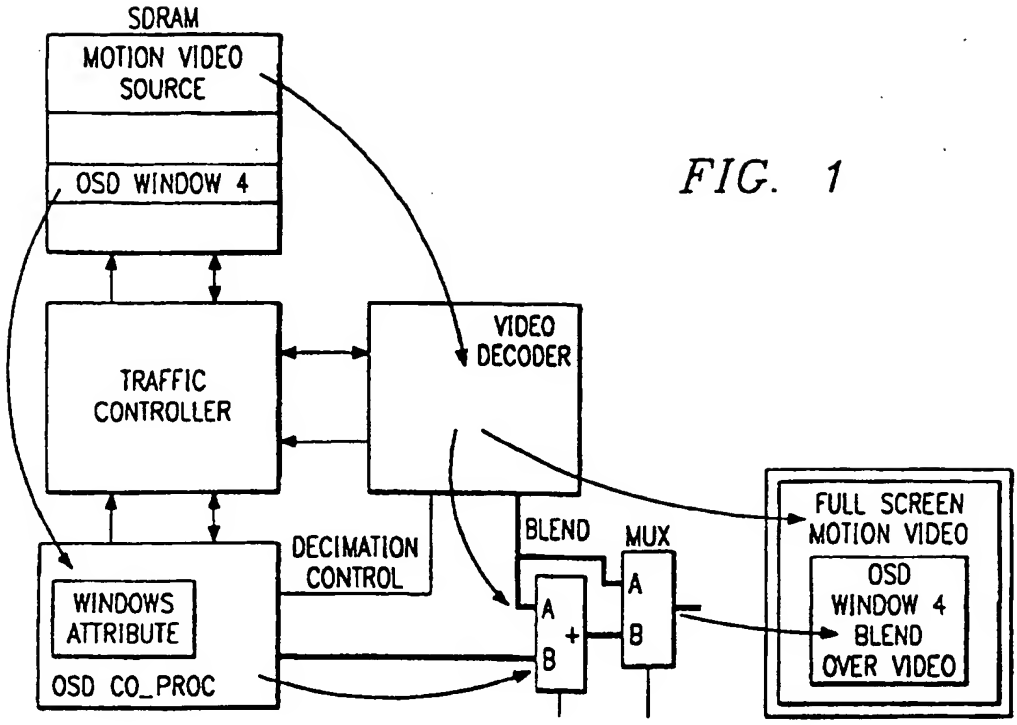

SDRAM
MOTION VIDEO SOURCE
OSD WINDOW 4
TRAFFIC CONTROLLER
VIDEO DECODER
DECIMATION CONTROL
BLEND
MUX
A
B
+
FULL SCREEN MOTION VIDEO
OSD WINDOW 4 BLEND OVER VIDEO
WINDOWS ATTRIBUTE
OSD CO_PROC

FIG. 1

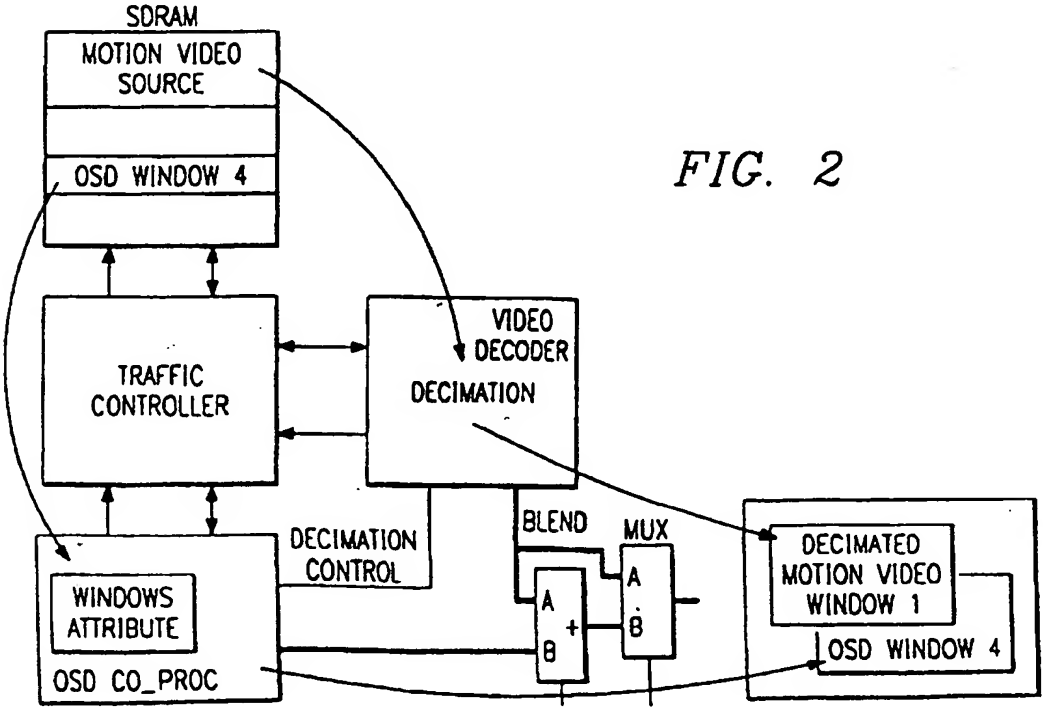

SDRAM
MOTION VIDEO SOURCE
OSD WINDOW 4
TRAFFIC CONTROLLER
VIDEO DECODER
DECIMATION
DECIMATION CONTROL
BLEND
MUX
A
B
+
DECIMATED MOTION VIDEO WINDOW 1
OSD WINDOW 4
WINDOWS ATTRIBUTE
OSD CO_PROC

FIG. 2

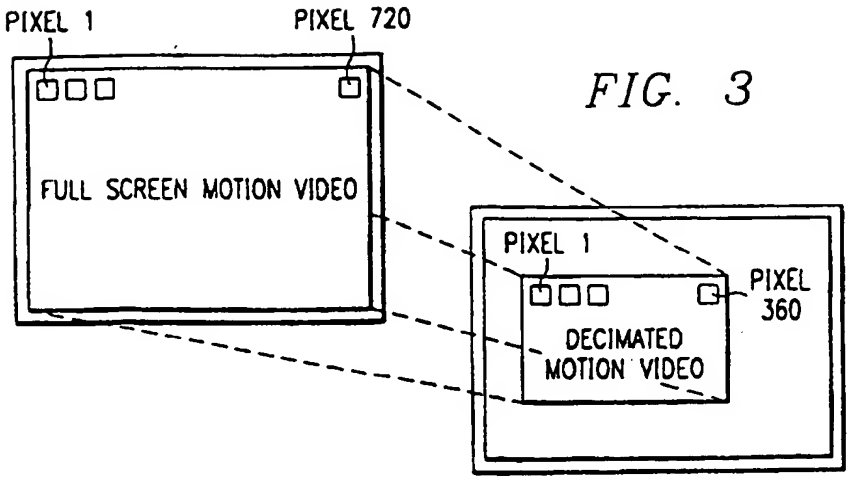


FIG. 3

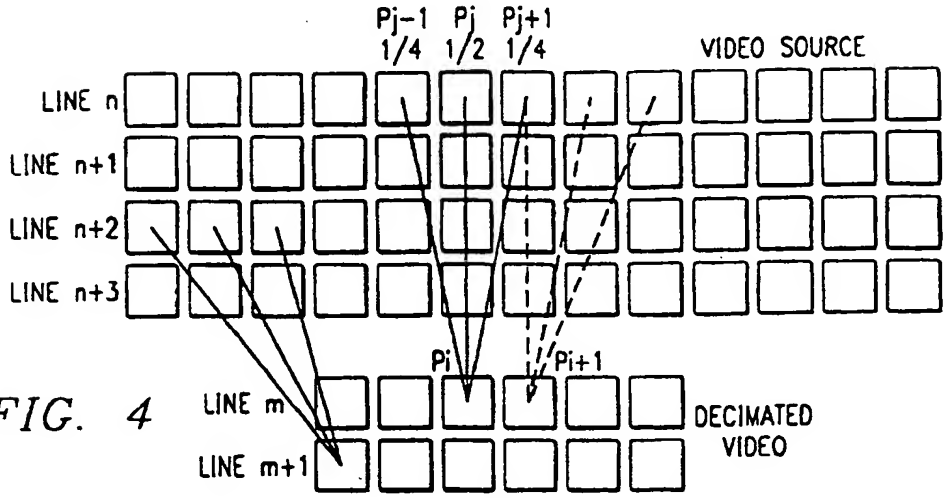


FIG. 4

OSD / VIDEO	OSD[7:0]	OSD[7:1]	OSD[7:1]+ OSD[7:2]	OSD[7:2]	0
VID[7:0]					FULL OSD
VID[7:1]		1/2 VIDEO 1/2 OSD			
VID[7:1]+ VID[7:2]				1/4 VIDEO 3/4 OSD	
VID[7:2]			3/4 VIDEO 1/4 OSD		
0	FULL VIDEO				

FIG. 8

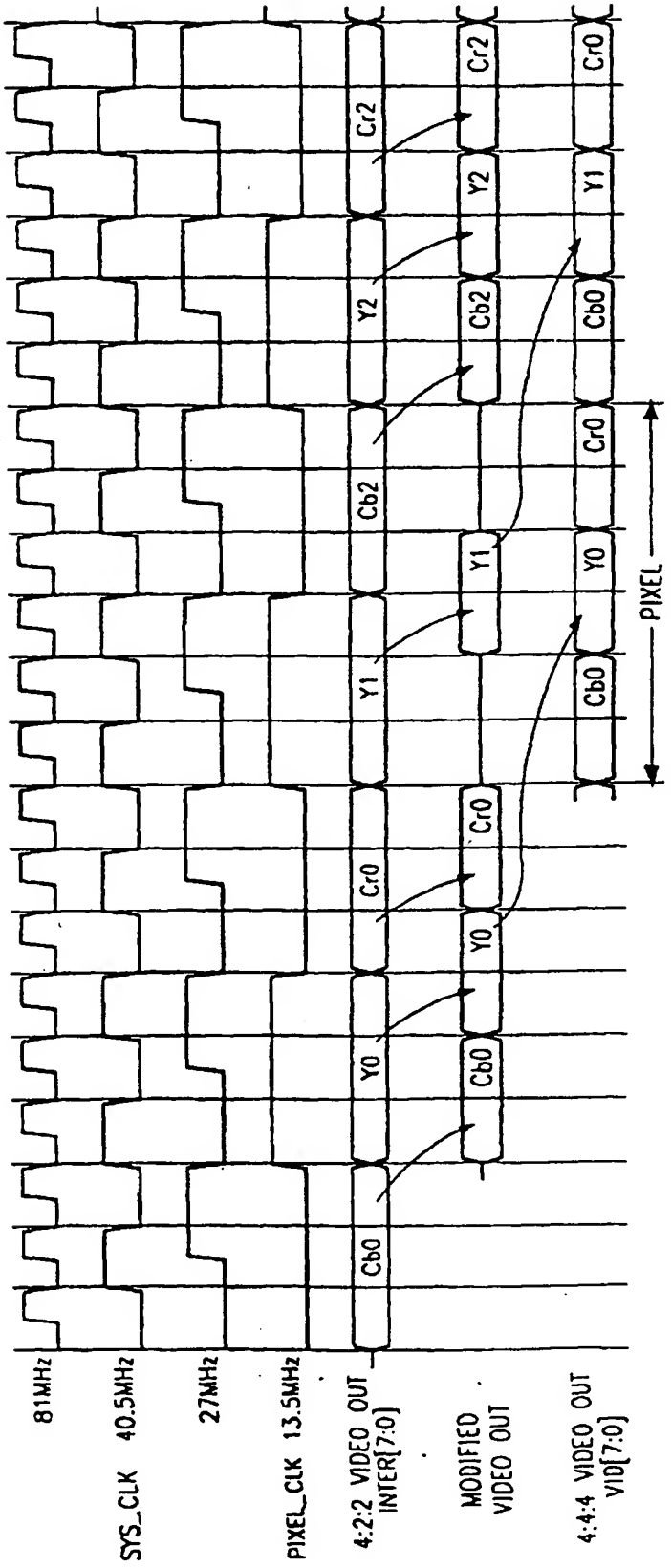

81MHz
SYS_CLK 40.5MHz
27MHz
PIXEL_CLK 13.5MHz
4:2:2 VIDEO OUT INTER[7:0]
MODIFIED VIDEO OUT
4:4:4 VIDEO OUT VID[7:0]
Cb0
Y0
Cr0
Y1
Cb2
Y2
Cr2
CbO
YO
CrO
PIXEL

FIG. 5

FIG. 6A

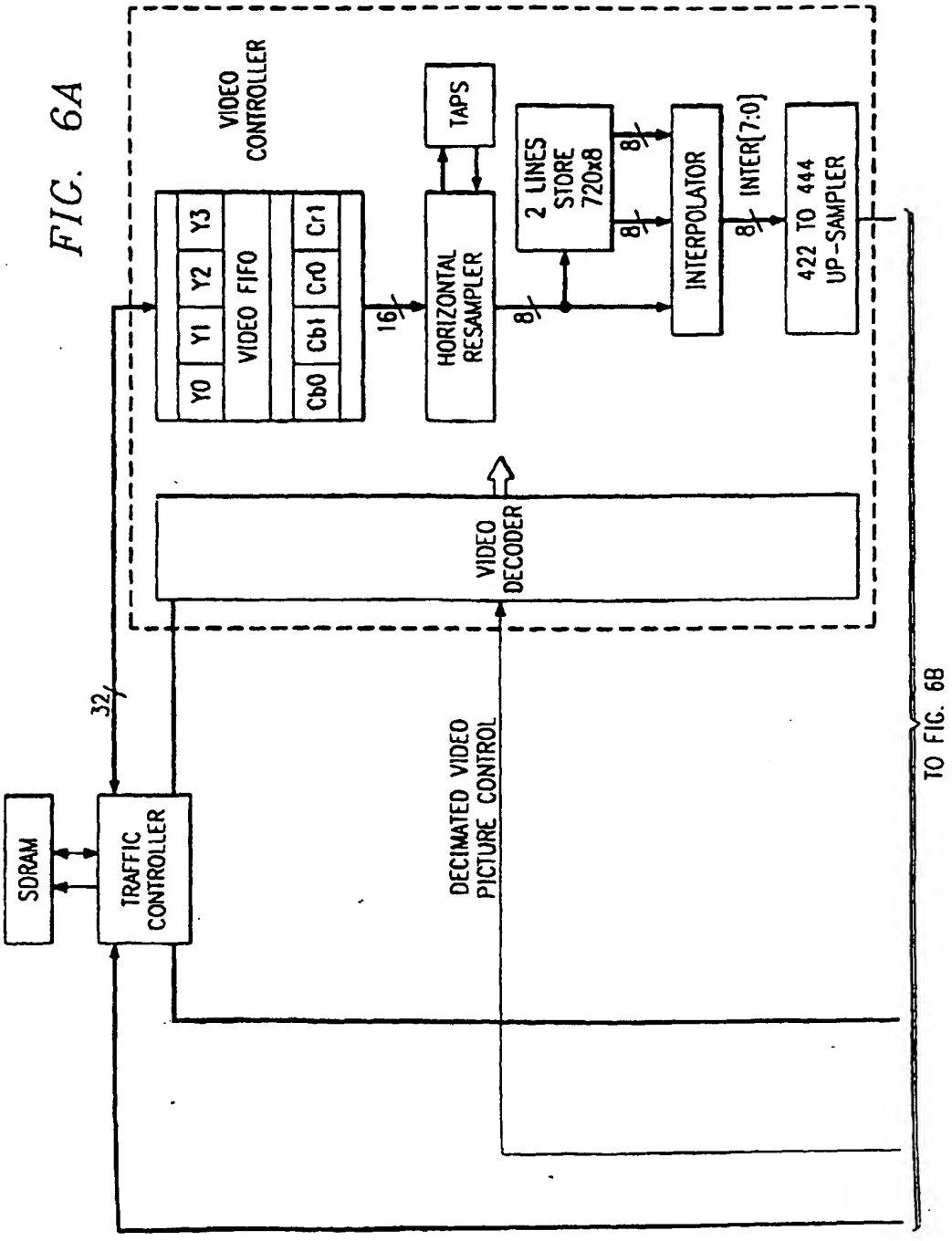

VIDEO CONTROLLER
VIDEO FIFO
Y0
Y1
Y2
Y3
Cb0
Cb1
Cr0
Cr1
16
TAPS
HORIZONTAL RESAMPLER
8
2 LINES STORE 720x8
8
8
INTERPOLATOR
8
INTER[7:0]
422 TO 444 UP-SAMPLER
VIDEO DECODER
32
SDRAM
TRAFFIC CONTROLLER
DECIMATED VIDEO PICTURE CONTROL
TO FIG. 6B

FIG. 6B

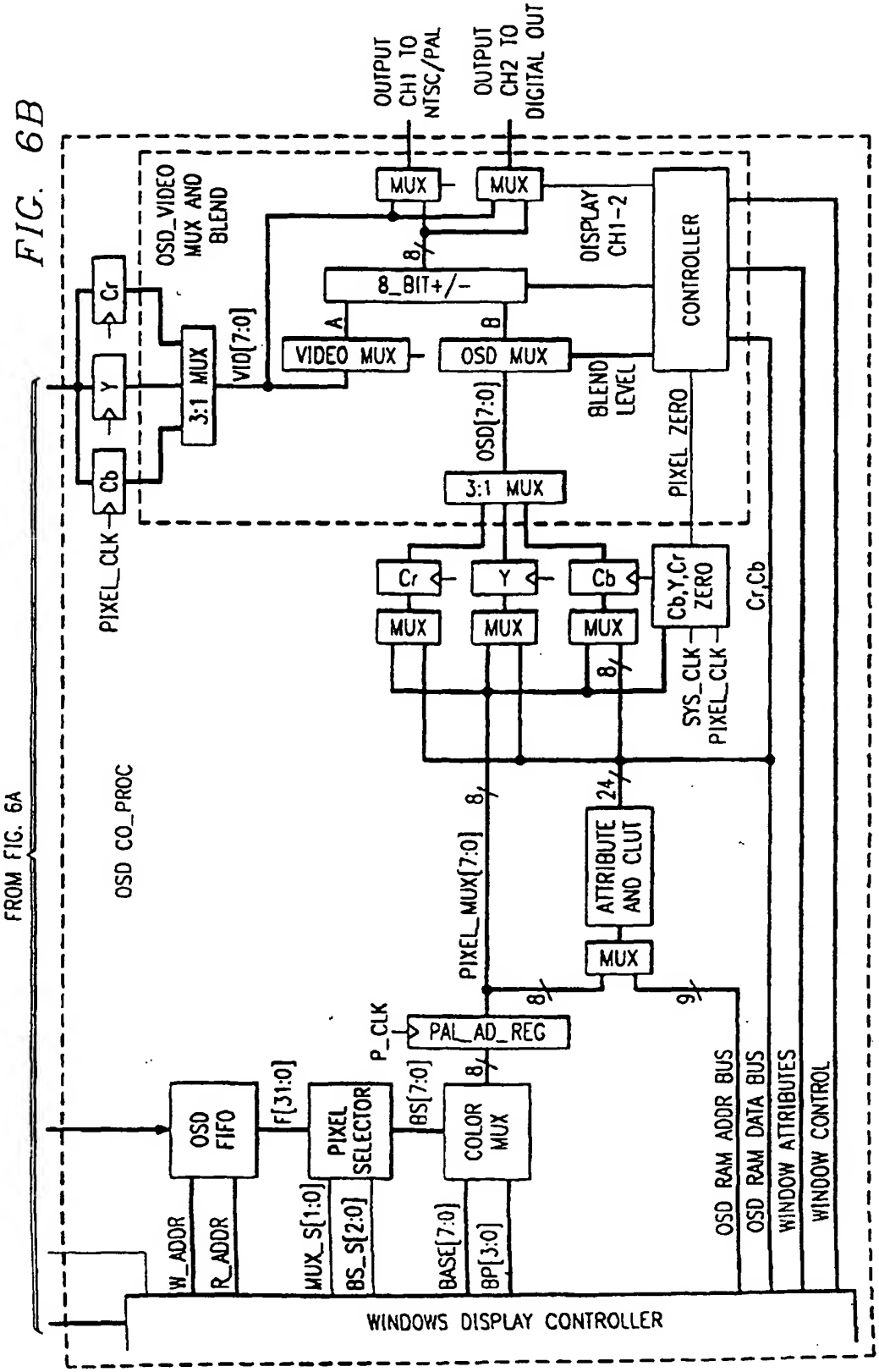
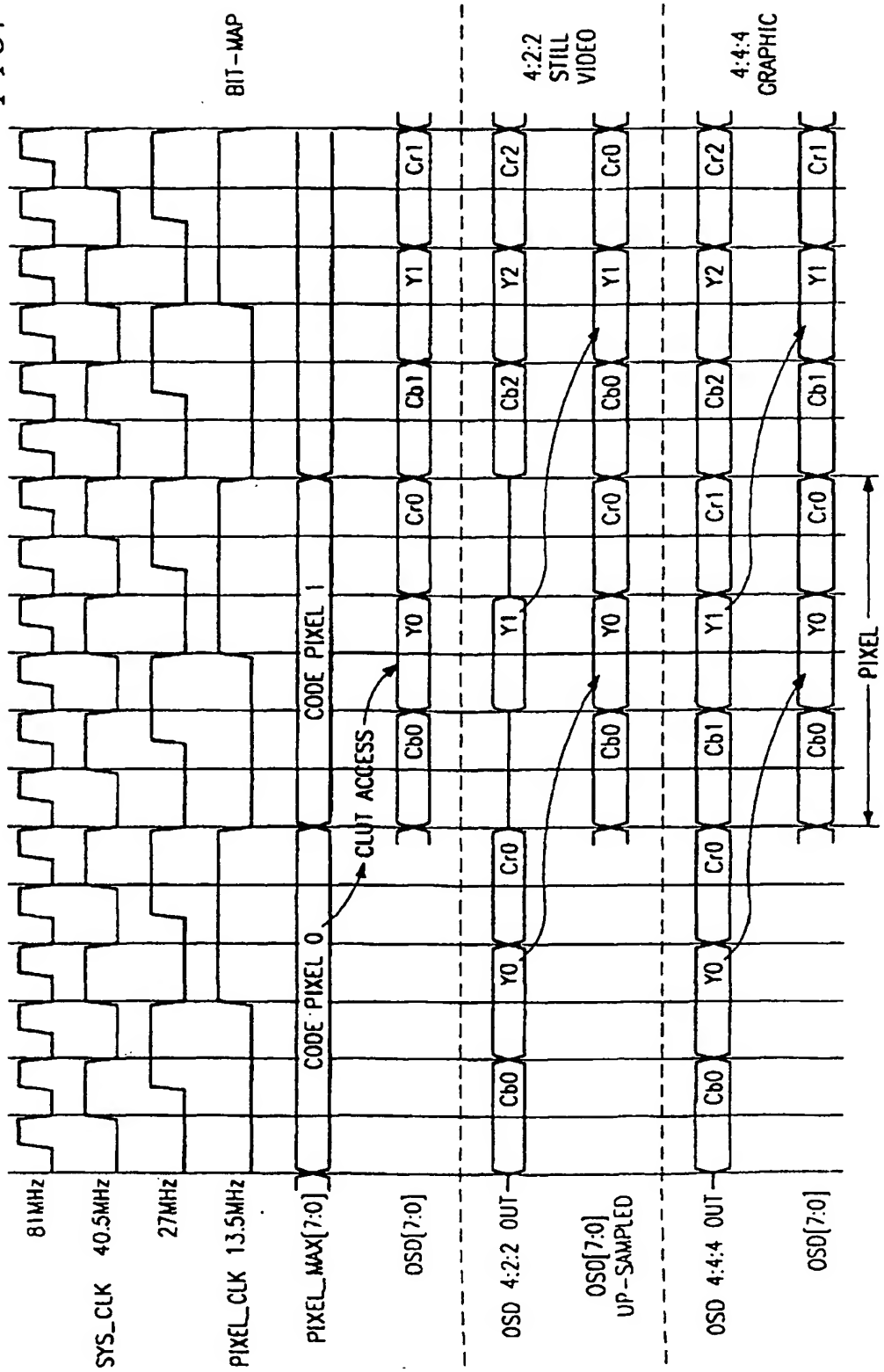

FROM FIG. 6A
OSD CO_PROC
OSD_VIDEO MUX AND BLEND
OUTPUT CH1 TO NTSC/PAL
OUTPUT CH2 TO DIGITAL OUT
MUX
DISPLAY CH1-2
CONTROLLER
8_BIT+/-
A
B
VIDEO MUX
OSD MUX
BLEND LEVEL
PIXEL ZERO
Cr
Y
Cb
3:1 MUX
VID[7:0]
OSD[7:0]
PIXEL_CLK
Cb,Y,Cr ZERO
Cr,Cb
SYS_CLK
PIXEL_CLK
PIXEL_MUX[7:0]
ATTRIBUTE AND CLUT
24
9
P_CLK
PAL_AD_REG
OSD FIFO
F[31:0]
PIXEL SELECTOR
BS[7:0]
COLOR MUX
W_ADDR
R_ADDR
MUX_S[1:0]
BS_S[2:0]
BASE[7:0]
BP[3:0]
OSD RAM ADDR BUS
OSD RAM DATA BUS
WINDOW ATTRIBUTES
WINDOW CONTROL
WINDOWS DISPLAY CONTROLLER

FIG. 7


81MHz
SYS_CLK 40.5MHz
27MHz
PIXEL_CLK 13.5MHz
PIXEL_MAX[7:0]
BIT-MAP
CODE PIXEL 0
CODE PIXEL 1
CLUT ACCESS
OSD[7:0]
OSD 4:2:2 OUT
4:2:2 STILL VIDEO
OSD[7:0] UP-SAMPLED
OSD 4:4:4 OUT
4:4:4 GRAPHIC
OSD[7:0]
PIXEL
Cb0
Y0
Cr0
Y1
Cb1
Y2
Cr1
Cb2
Cr2

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 840 505 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
29.12.1999 Bulletin 1999/52

(43) Date of publication A2:
06.05.1998 Bulletin 1998/19

(21) Application number: **97119124.2**

(22) Date of filing: **03.11.1997**

(51) Int. Cl.[6]: **H04N 5/45**

(84) Designated Contracting States:
AT BE CH DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

(30) Priority: **01.11.1996 US 30104 P**

(71) Applicant:
TEXAS INSTRUMENTS INCORPORATED
Dallas, Texas 75243 (US)

(72) Inventors:
- **Chauvel, Gerard**
  06600 Antibes (FR)
- **Chae, Brian**
  Plano, TX 75075 (US)

(74) Representative: **Holt, Michael**
Texas Instruments Limited,
P.O. Box 5069
Northampton NN4 7ZE (GB)

(54) System to multiplex and blend graphics OSD and motion video pictures for digital television

(57) A system is provided to multiplex graphic and Motion video pictures for digital TV set-top box. The motion picture is generated by an MPEG Video decoder and the graphic windows are generated by an OSD Co-Processor. Each graphic window is characterized by a set of attributes that define the display mode, position on the screen, priority and blend factor. When a window is blended, the motion video and OSD color components are added together with a proportion of each defined by the window attributes. Decimated motion video picture can be also displayed within an OSD window; the OSD Co-processor generates an empty window that is filled by the video decoder with the decimated motion video.

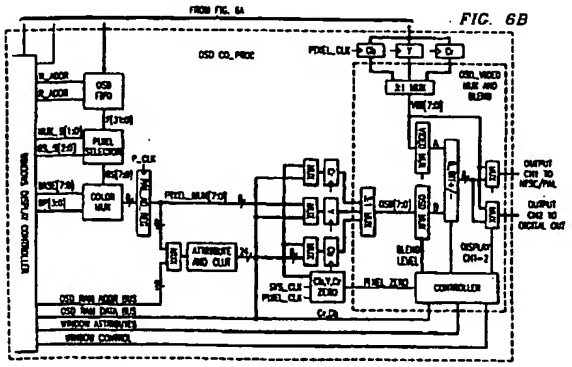


FIG. 6B

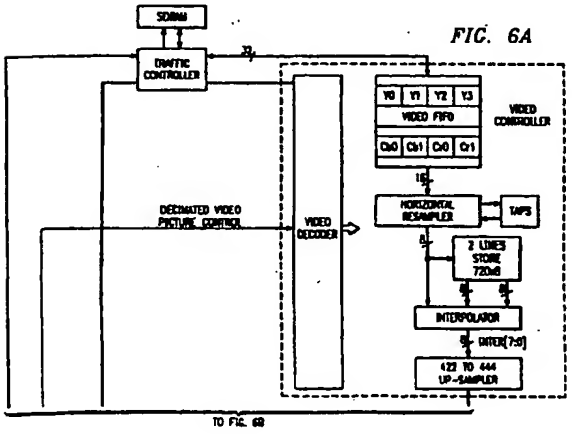


FIG. 6A

EP 0 840 505 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 9124

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 534 942 A (BEYERS JR BILLY W ET AL) 9 July 1996 (1996-07-09) * column 1, line 52 - column 2, line 3 * * column 2, line 24 - column 4, line 54; claim 1; figure 1 *	1,2	H04N5/45 H04N5/445
X	WO 96 18991 A (AURAVISION CORP) 20 June 1996 (1996-06-20) * page 1, line 1 - page 2, line 11; claim 1; figures 1-3 *	1,2	
A	EP 0 701 367 A (THOMSON CONSUMER ELECTRONICS) 13 March 1996 (1996-03-13) * column 1, line 56 - column 2, line 36; figure *	1,2	
A	US 4 680 629 A (FUKUSHIMA NOBUO ET AL) 14 July 1987 (1987-07-14) * the whole document *	1,2	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6) H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	11 November 1999	Fuchs, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 97 11 9124

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

11-11-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5534942 A	09-07-1996	BR 9508012 A	02-09-1997
		CA 2191556 A	28-12-1995
		CN 1152985 A	25-06-1997
		DE 69505668 D	03-12-1998
		DE 69505668 T	08-04-1999
		EP 0765574 A	02-04-1997
		FI 965037 A	16-12-1996
		JP 10501943 T	17-02-1998
		WO 9535626 A	28-12-1995
WO 9618991 A	20-06-1996	US 5696527 A	09-12-1997
		US 5644325 A	01-07-1997
		US 5644333 A	01-07-1997
		US 5621428 A	15-04-1997
		AU 4413396 A	03-07-1996
		EP 0870295 A	14-10-1998
EP 0701367 A	13-03-1996	CA 2156871 A	10-03-1996
		CN 1138796 A	25-12-1996
		JP 8181955 A	12-07-1996
		SG 32490 A	13-08-1996
		US 5625406 A	29-04-1997
US 4680629 A	14-07-1987	JP 60180387 A	14-09-1985
		AU 570301 B	10-03-1988
		AU 3919885 A	05-09-1985
		CA 1212453 A	07-10-1986
		EP 0154301 A	11-09-1985

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82